FIG.1

Figure 2

300

302

A/D Converters

Video Scaling

XGA RGB (0 : 17)

304 Mother Board

RGB to CMP-FED video converter

Analog RGB

RGB (0 : 35)

Pwm (0:192)

306 Column Modules

CMP-FED video to PWM converter

Pwm (2880:3071)

308 MTI CMP-FED column drivers

32 Flex Connections

310 MTI CMP-FED

8 Flex Connections

312 Row Scan Drivers

DISPLAY
CONNECTOR

408

DRIVER
CIRCUITRY

308

PWM
CIRCUITRY

306

DATA INPUT
CONNECTOR -

402

400

Figure 3

ODD COLUMNS

	1	2	3	4	5	6	7
COL_ADD = 0	129 — 255	257 — 383	385 — 511	513 — 639	641 — 767	769 — 895	897 — 1023
1 — 127, K07 512, Xilinx 510, 506	506	506	506	506	506	506	506

EVEN COLUMNS

	1	2	3	4	5	6	7
Xilinx, K07 508	508	508	508	508	508	508	508
COL_ADD = 0, 1 — 128	130 — 256	258 — 384	386 — 512	514 — 640	642 — 768	770 — 896	898 — 1024
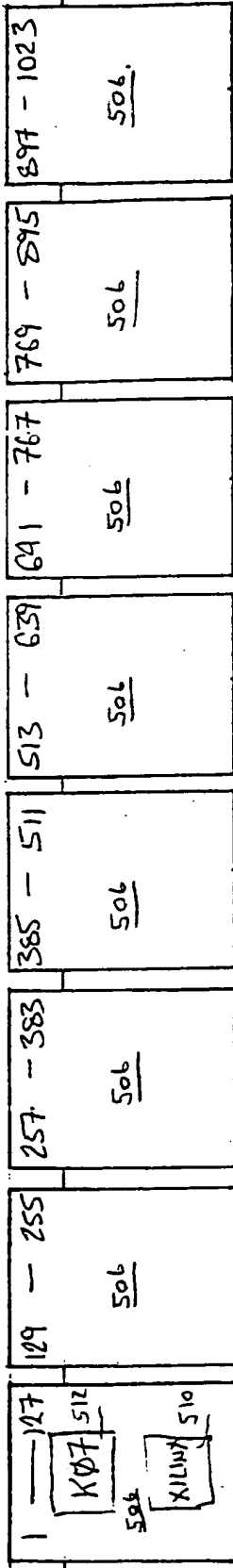
DIODE TERMINATING BUFFERS

502a, 502b, 504a, 504b

J1

RGB ODD
O-PLCK
COL_ADD[0:2]
+3.3v, +5v
HSYNC/OSYNC

502c, 502d, 504c, 504d

J2

RGB EVEN
E-PLCK
COL_ADD[0:2]
+3.3v, +5v
HSYNC, VSYNC

ROW-DATA
ROW-CLK

60-WIRE TWISTED-PAIR RIBBON CABLE

SAME
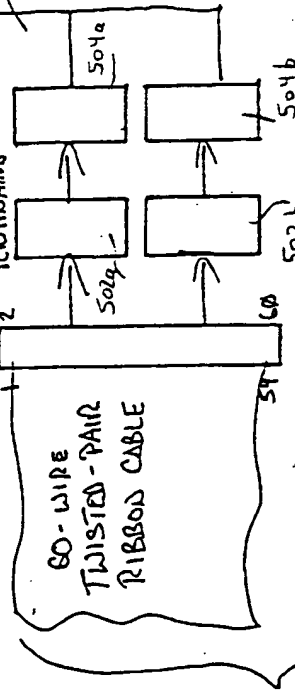
FROM SECOND VIDEO CIRCUITRY 304

Figure 4
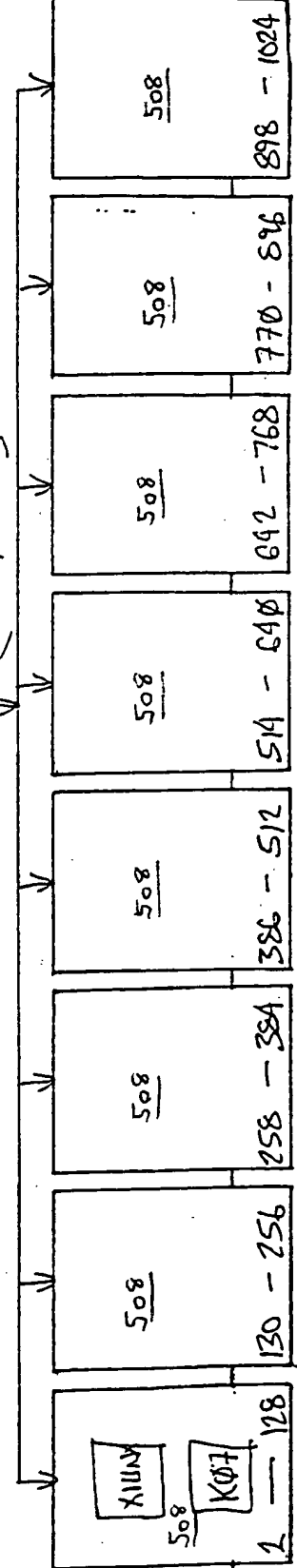
512 ⟶

606a 48 bit Latch and HV line Driver	Outputs (0 : 47)
48 bit Latch and HV line Driver	Outputs (48 : 95) 606b
48 bit Latch and HV line Driver	Outputs (96 : 143) 606c
48 bit Latch and HV line Driver	Outputs (144 : 191) 606d

1 bit HV Refresh 610

4 bit Latch Enable Buffer 608a

48 bit Buffer 604

602

DATA BUS ⟶
LATCH
ENABLES

H V INPUT (up to 80 v max ; 60 nominal)

Figure 5

Figure 6

512

48bit Reg3/HVOUT

48bit Reg2/HVOUT

48bit Reg1/HVOUT

HVGATE

48bit Reg0/HVOUT

DFF + "WIRED-OR'ed" OUTPUTS

DATA

CLK

HVOUT (1 of 192)

INPUT BUS (48)

INPUT PROTECT

I BUFFERS

CLKx4

DATA
BUS 　　　　〈0:47〉〈48:95〉〈9̇ : 143〉〈144:191〉

LE0

LE1

LE2

LE3
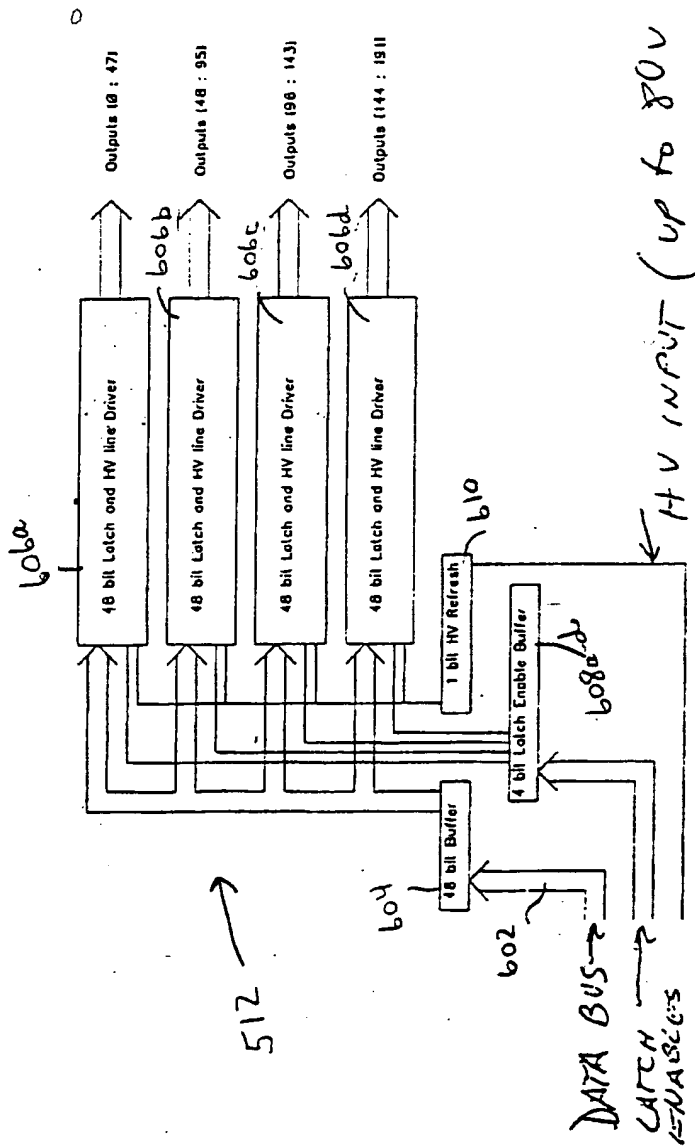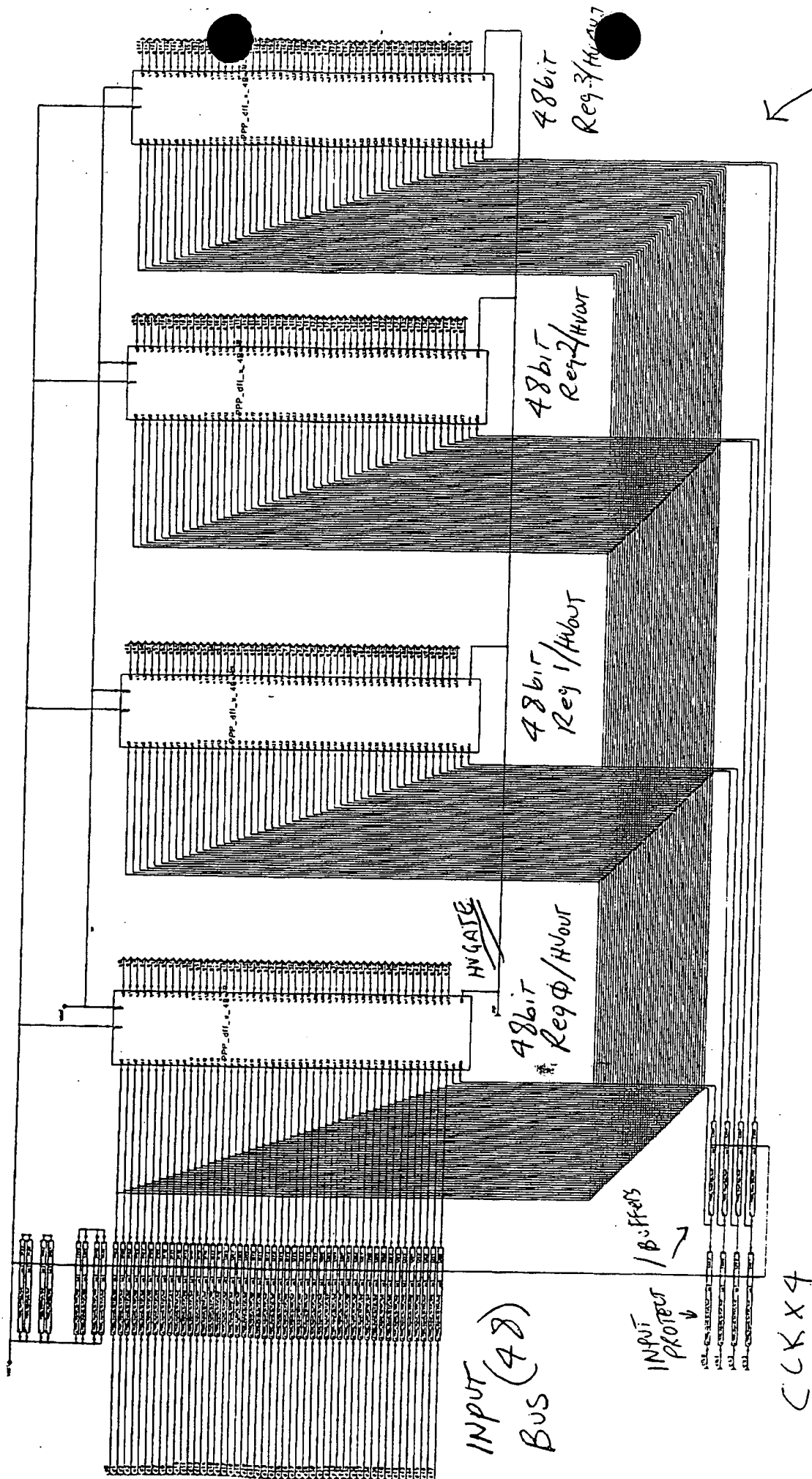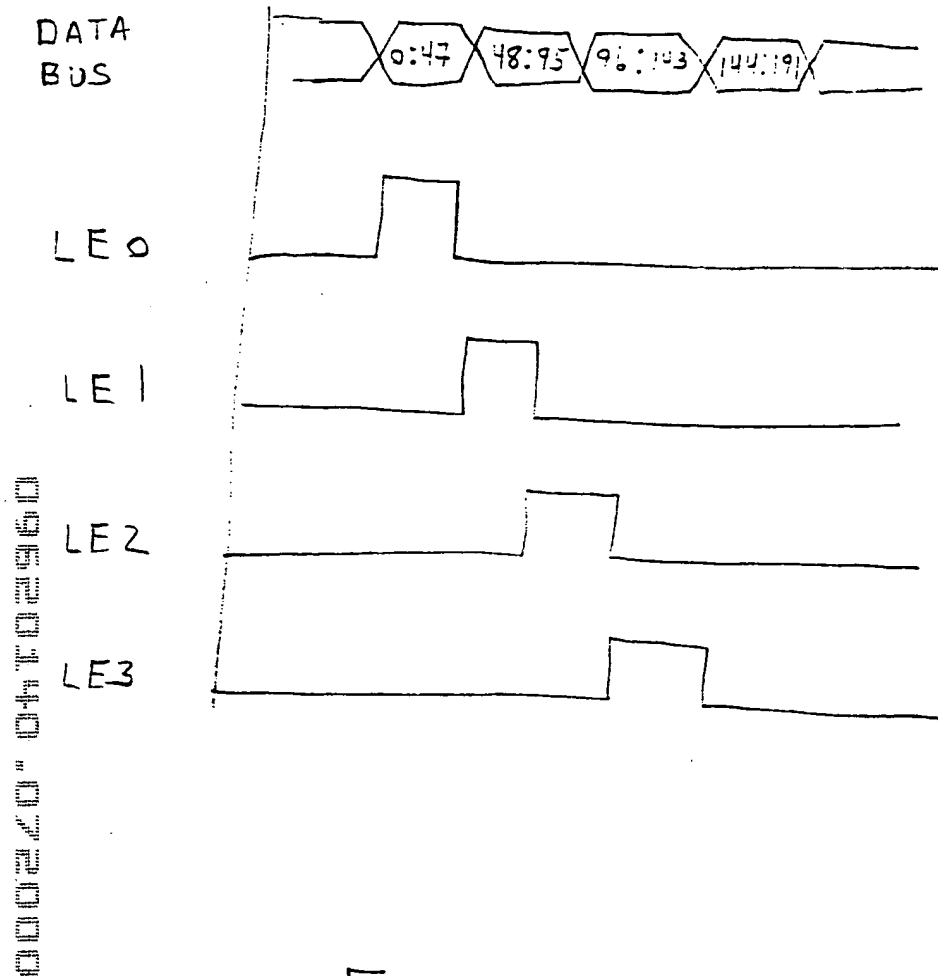
Figure 7

VIDEO TIMING (BASED ON VESA 1024 × 768 @ 60 Hz STANDARD)
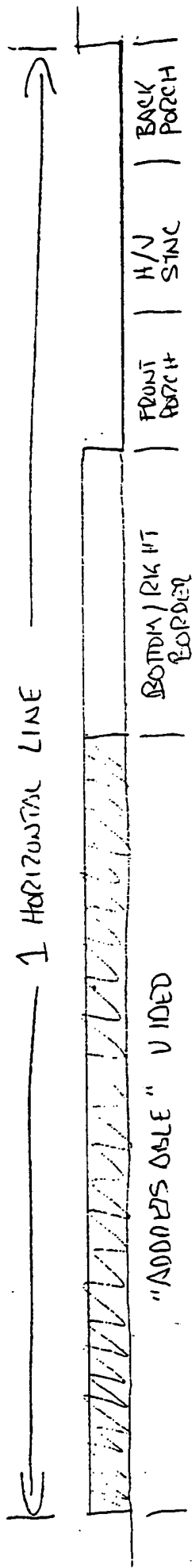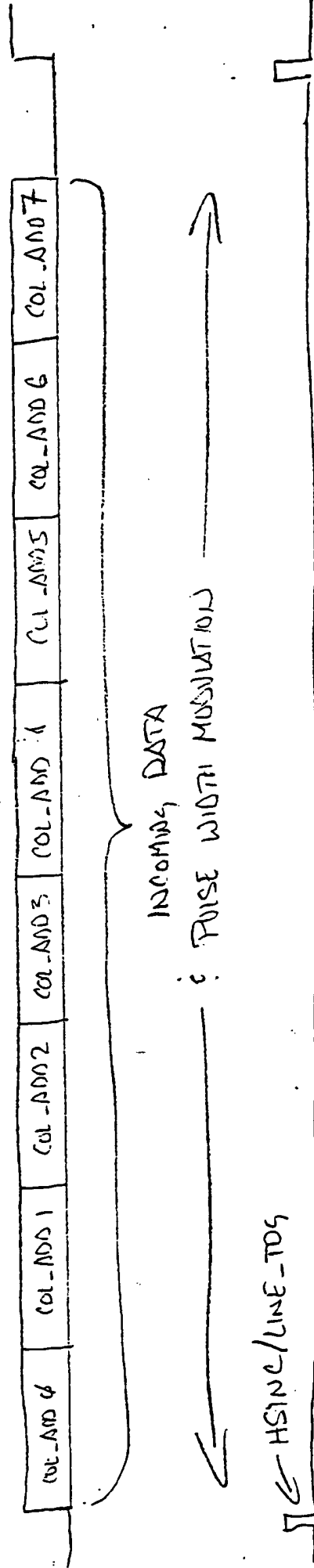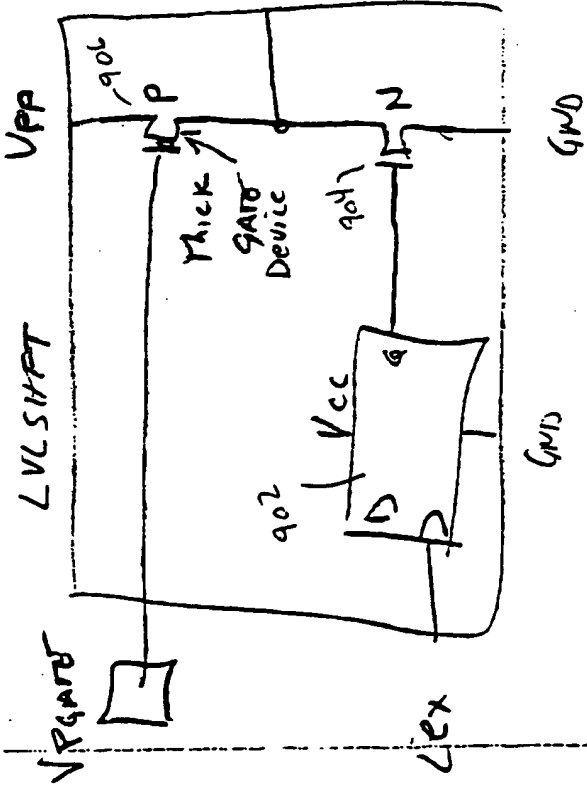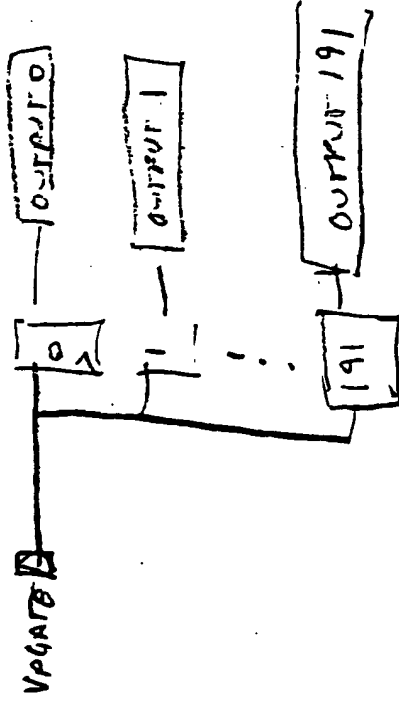
1 HORIZONTAL LINE

"ADDRESSABLE" VIDEO | BOTTOM/RIGHT BORDER | FRONT PORCH | H/V SYNC | BACK PORCH

DIGITAL TIMING

| COL_ADD 0 | COL_ADD 1 | COL_ADD 2 | COL_ADD 3 | COL_ADD 4 | COL_ADD 5 | COL_ADD 6 | COL_ADD 7 |

INCOMING DATA

? PULSE WIDTH MODULATION

HSYNC/LINE_TDS

Figure 8

Figure 9A

LVLSHFT V_{PP}

P — 906

Thick GATE Device

N

907 — 904

V_{cc} 902

GND

Vex GND

V_{PGATE}

OUTPUT

Figure 9B

V_{PGATE}

0 → OUTPUT 0

1 → OUTPUT 1

191 → OUTPUT 191

Figure 9C

$V_{PP} - vr$

V_{PGATE} "0"

pull all outputs high during Refresh

Figure 9D

V_{DATA}

PWM

min

HALF

FULL BRIGHT

turn all N channels off for refresh

DATA
IN

DATA
OUT

Figure 10A

0V

DATA
IN

DATA
OUT

+V
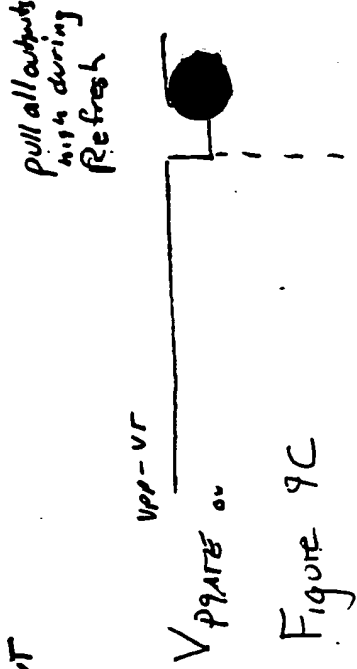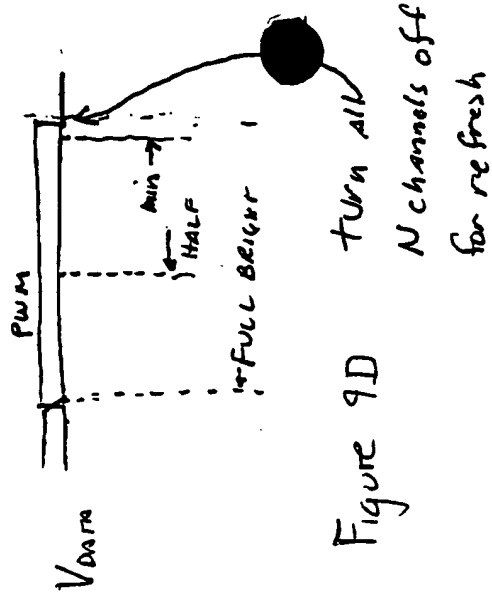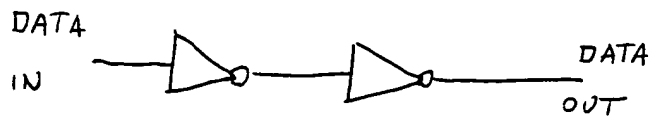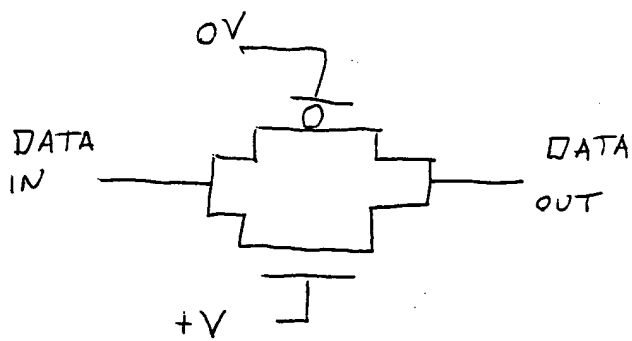
Figure 10B

$$\tau\ \text{VIDEO DATA} <= \frac{1}{\#\text{Rows} \cdot \#\text{Refres}} = \frac{1}{768 \cdot 72} < 18\mu S$$

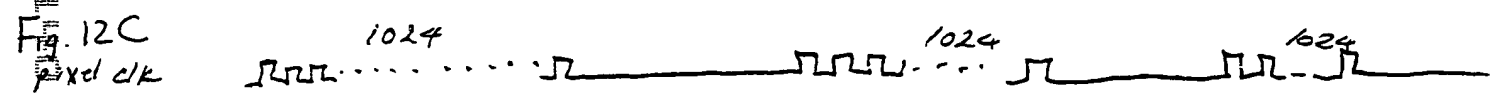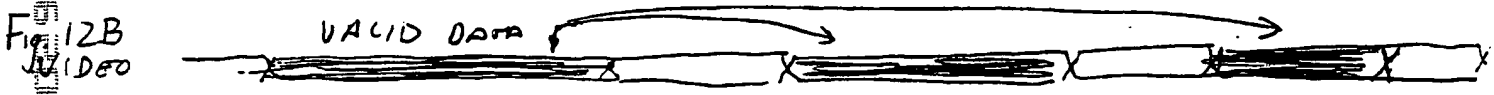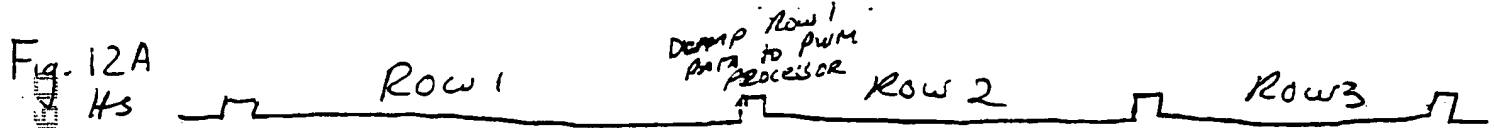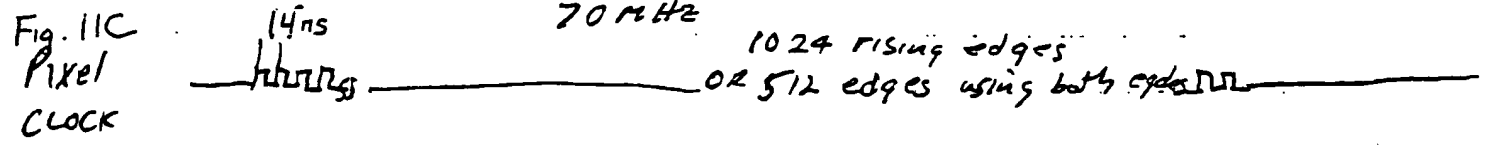use this full 18μs — standard valid video will be about 80% or 14.5 μs

Fig. 11A
HS

for example 14.5μs

Fig. 11B
VIDEO

1024 columns

Fig. 11C
Pixel
CLOCK

14ns   70 MHz   1024 rising edges
or 512 edges using both edges

Fig. 12A
HS

Row 1   DUMP Row 1 to PWM data to processor   Row 2   Row 3

Fig. 12B
VIDEO

VALID DATA

Fig. 12C
pixel clk

1024   1024   1024

video to PWM clk

DRIVE ROW 1 on DISPLAY
256

pw

Fig. 12D

510   512

EQUIVALENT SCHEMATIC

SLAVE DISPLAY DRIVER CHIP

PWM CLK
VIDEO DATA
Pixel CLK

1304a   1306a   1308

98-35? LOADABLE DOWN COUNT   48 COMP

1304b   1306b

LOADABLE DOWN COUNT   48 COMP

1304c   1306c

48 COMP

1024

M U X

48
4E
4

0:47

606a   48   95

606b

606c   96

606d   143

1304d   1306d

48

144 191

Fig. 13

HS
PARALLEL DUMP